# High-Gain Transimpedance Amplifier in InP-Based HBT Technology for the Receiver in 40-Gb/s Optical-Fiber TDM Links

Jens Müllrich, Herbert Thurner, Ernst Müllner, Joseph F. Jensen, *Senior Member, IEEE*, William E. Stanchina, *Member, IEEE*, M. Kardos, and Hans-Martin Rein, *Senior Member, IEEE*

***Abstract*—A monolithic integrated transimpedance amplifier for the receiver in a 40-Gb/s optical-fiber TDM system has been fabricated in an InP-based HBT technology. Despite its high gain (transimpedance of 2 kΩ in the limiting mode, 10 kΩ in the linear mode) the complete amplifier was realized on a single chip. Clear output eye diagrams were measured up to 43 Gb/s under realistic driving conditions. The voltage swing of 0.6 $V_{pp}$ at the differential 50 Ω output does not change within the demanded input dynamic range of 6 dB. At the upper input current level even 48 Gb/s were achieved. The power consumption is approximately 600 mW at a single supply voltage of −5.5 V.**

***Index Terms*—Compound semiconductors, HBT circuits, optical communication ICs, transimpedance amplifier.**

## I. Introduction

FUTURE optical-fiber TDM (time division multiplexing) links will operate at data rates of 40 Gb/s. To achieve this aim, sophisticated technologies for the opto-electronic and electronic components are required and an adequate system concept must be used [1].

The scheme of a 40-Gb/s link is shown in Fig. 1. In the receiver of this link, a gain controlled optical amplifier (OA) is used in front of a high-current photodiode (PD). As a consequence, the input sensitivity, dynamic range, and total gain of the amplifier can be reduced compared to systems without OA's [1]. Here, the output signal of the amplifier is time-regenerated by the first stage of a demultiplexer ("decision DEMUX") rather than by a single master–slave D-flip-flop. By this measure, the clock-phase margin and input sensitivity are essentially improved and the clock frequency to be extracted is halved (20 GHz).

Nevertheless, the transimpedance amplifier in the receiver is one of the most speed-critical components of the system. As a consequence of the reduced total gain in the receiver (due to the use of an optical amplifier), a separation into a pre- and main-amplifier chip proved no longer to be required, thus reducing costs and avoiding critical interfaces [2].

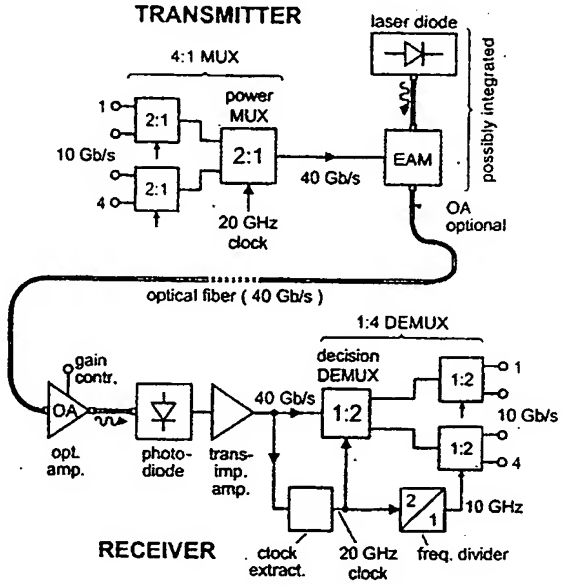


Fig. 1. Scheme of a 40 Gb/s optical-fiber TDM link [1].

In this paper, a single-chip transimpedance amplifier in InP-based HBT technology developed for an advanced 40-Gb/s system, is presented. Despite the comparatively high gain, it operates reliably up to 43 Gb/s within the dynamic range of interest and is, thus, faster than the 40-Gb/s SiGe amplifier published two years ago [2]. The output voltage swing is high enough to drive both the succeeding decision circuit and the clock recovery circuit directly via matched 50-Ω transmission lines.

## II. Circuit Design

Fig. 2 shows the block diagram of the transimpedance amplifier. The circuit consists of three cascaded amplifier cells, discussed below. Differential operation is consequently applied. Besides other advantages, this operation mode reduces noise problems, typical in amplifiers with such a high gain and operating speed (cf. Section III).

Comprehensive investigations of different amplifier concepts have shown that the required high gain can hardly be achieved with a completely linear circuit at the required high operating speed. Therefore, only the first amplifier cell operates in the

Manuscript received January 18, 1999; revised March 27, 2000.

J. Müllrich and H.-M. Rein are with Ruhr-University Bochum, D-44780 Bochum, Germany (e-mail: rein@aghl.ruhr-uni-bochum.de).

H. Thurner was with Siemens AG, Munich, Germany. He is now with the University of Applied Science, D-83024 Rosenheim, Germany.

E. Müllner is with Siemens AG, Information and Communication Networks, D-81359 Munich, Germany.

J. F. Jensen, W. E. Stanchina, and M. Kardos are with HRL Laboratories, Malibu, CA 90265 USA.

Publisher Item Identifier S 0018-9200(00)05916-3.

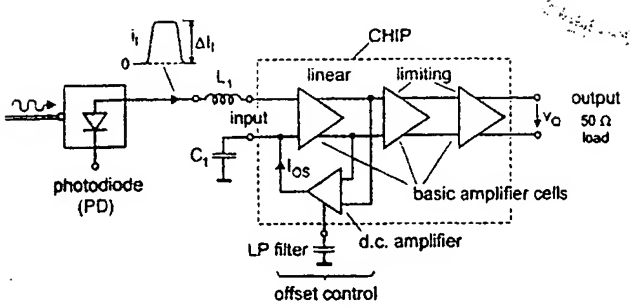


Fig. 2. Simplified block diagram of the limiting transimpedance amplifier ($L_1$ = adjusted input bond inductance, $C_1$ = off-chip decoupling capacitor).

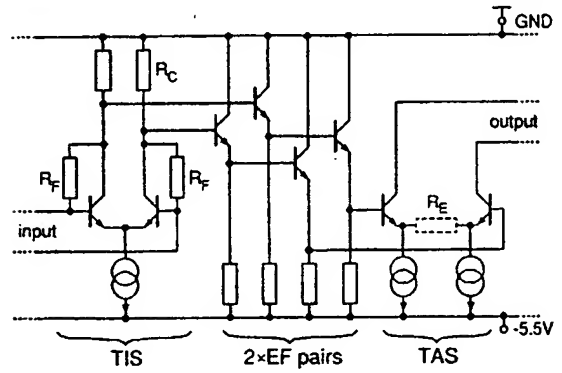


Fig. 3. Basic amplifier cell. In the first and second cell, $R_E$ is replaced by a short.

linear and the others in the limiting mode. The limiting mode guarantees the desired constant output swing and, in addition, compensates the gain drop at high frequencies.

An important design aspect for this separation into a linear and a limiting part is as follows. The group delay of the first (linear) amplifier cell should deviate only weakly from the (constant) low-frequency value up to high frequencies, since this deviation would result in time jitter which can hardly be regenerated by the succeeding limiting cells. In contrast, a drop in signal amplitude of the first cell with increasing frequency can be compensated by amplitude limitation in the succeeding cells. Therefore, the first (linear) cell of this amplifier shows a lower cutoff frequency for the magnitude compared to the phase.

The simplified circuit diagram of the (linear and limiting) amplifier cells is shown in Fig. 3. Each cell consists of a transimpedance stage (TIS), succeeded by two emitter follower pairs (EF) and a transadmittance stage (TAS). The negative-feedback resistor $R_E$ is only used in the third stage to reduce potential ringing. Note, that at each interface between succeeding amplifier stages the principle of strong mismatching is met [3].

The currents of the TIS and TAS as well as of the second EF pair are adjustable (via additional bond pads) for compensation of potential spread in technology and model parameters. Apart from $R_E$ and from the bias currents and dimensions of the transistors, there are only slight distinctions between the different cells (e.g. the feedback resistance $R_F$ varies between 200 and 400 Ω).

Since the driving PD is dc coupled to the input of the amplifier (Fig. 2), an automatic offset control is required to compensate the offset of the input signal current (i.e. half of the input current swing $\Delta I_I$). This offset control consists of an on-chip dc amplifier and an external capacitor for lowpass (LP) filtering. The current generated by the offset control as well as an additional current for optional fine-adjustment of the input threshold with respect to minimum bit error rate (not shown in Fig. 2) are fed into the complementary input of the first differential transimpedance stage, which is decoupled by an off-chip capacitor ($C_1$). This capacitor additionally reduces the influence of the shot-noise, mainly caused by the output current source in the offset control circuit. The control signal is picked off at the output of the first EF pair in the first amplifier cell.

While the bond inductance to the decoupling capacitor $C_1$ has to be as low as possible, the input bond inductance $L_1$ is optimized mainly with respect to optimum frequency response by adjusting the bond length. The optimal value is about 0.4 nH, corresponding to a bond length of 0.5 mm. In order to reduce potential double reflections between the amplifier output and the succeeding circuits which are driven by 50-Ω microstrip lines, two on-chip output resistors (60 Ω) are used which, however, increase the current to be switched by the output stage.

A constant differential output voltage swing of $\Delta V_Q = 600$ $mV_{pp}$ at 50 Ω external load must be achieved at an input current swing $\Delta I_I$ between 0.3 and 0.6 $mA_{pp}$ (6 dB electrical dynamic range).[1] Thus, the total transimpedance, i.e. the output voltage swing related to the (minimum) input current swing, is $Z_{TI} \approx 2$ kΩ in the limiting mode (small-signal value about 10 kΩ). The simulated equivalent input noise current density averaged over the frequency range of interest (≈20 pA/$\sqrt{\text{Hz}}$) proved to be well below the system requirements (≤25 pA/$\sqrt{\text{Hz}}$). Due to the on-chip output termination (60 Ω) the effective load is 27.3 Ω, so that the output stage has to switch 11 mA.The total power consumption is about 600 mW at a single supply voltage of $V_0 = -5.5$ V.

## III. Layout Considerations

Amplifiers with such a high gain and operating speed must be designed very carefully [3]. This holds not only for the optimization of the transistor sizes and resistances but also for the arrangement of the amplifier stages on the chip and for the on-chip wiring. For example, critical lines must be shortened at the cost of uncritical ones. Longer lines were designed as microstrip lines with the lower metallization layer used as a ground plane.

Due to the great influence of the layout and mounting parasitics, the circuit simulation must be closely related to the layout and to the mounting technique. For this, on-chip wiring parasitics were extracted and introduced into the simulation (cf. Section V). This holds for the longer lines between the amplifier cells (simulated as coupled microstrip lines) and for the short interconnections between the circuit components within an amplifier cell, as well as for the connections from the cells to the ground and supply voltage pads. The bond inductances (including the mutual inductances) were calculated by use of an adequate computer program.

[1]This voltage swing is high enough to drive both the succeeding decision DEMUX and the clock recovery circuit via a passive power divider (cf. Fig. 1).

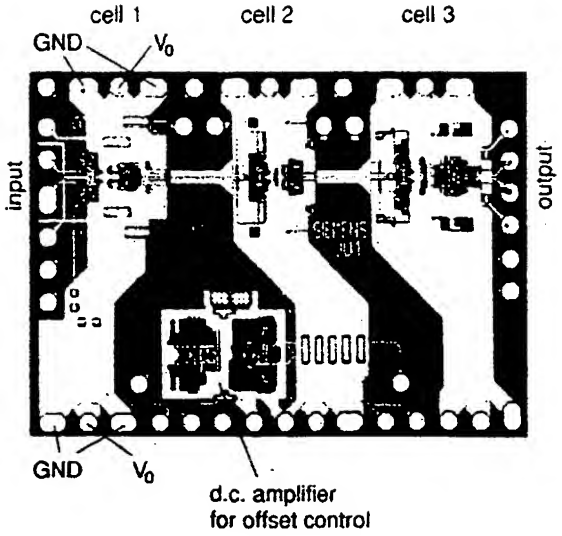


Fig. 4. Chip photograph of the transimpedance amplifier. The chip size is 1.6 mm × 1.2 mm. The pads for ground (GND) and supply voltage ($V_0$) are only marked in the first amplifier cell.

A problem of the single-ended amplifier input is its sensitivity to common-mode noise. Due to the different off-chip impedances at both nodes of the input (comparatively high at the used input terminal and low at the ac decoupled terminal), potential common-mode noise is transformed into differential noise, which is added to the data signal and results in ringing and time jitter. The common-mode noise may be generated by the amplifier cells themselves (especially by the switching of the EF's in the limiting cells) or may originate from external influences (e.g. from an insufficient common-mode reflection coefficient at the inputs of the succeeding circuits). To minimize the interaction of these noise sources with the sensitive amplifier input (e.g. via the parasitic inductances of common on-chip lines and bonds to the ground and supply voltage terminals or via the substrate), the different amplifier cells were electrically and spatially separated by adequate measures in the layout. For example, separate ground and supply-voltage pads for each cell are required. The wide distance between the amplifier cells results in comparatively long signal lines, which, however, can be tolerated as long as the lines are driven by the (high-impedance) output of a TAS [3]. However, the efficient shielding of the two input pads by a low-ohmic buried layer, used e.g. in the amplifier described in [2], is not possible with the technology used here.

Careful simulations supported by the powerful substrate simulator SUSI [4], [5] proved these measures to be sufficient to guarantee reliable operation. However, it should be mentioned that the coupling between the cells via the semi-insulating substrate is not necessarily lower compared to an amplifier designed in a SiGe bipolar technology with its resistive (e.g. 20 Ωcm) substrate [2].

The chip photograph in Fig. 4 shows the three clearly separated amplifier cells, connected by comparatively long differential microstrip lines, and, moreover, the strictly symmetrical layout within the amplifier cells. Most of the bond pads are related to dc terminals which are provided for adjusting some bias

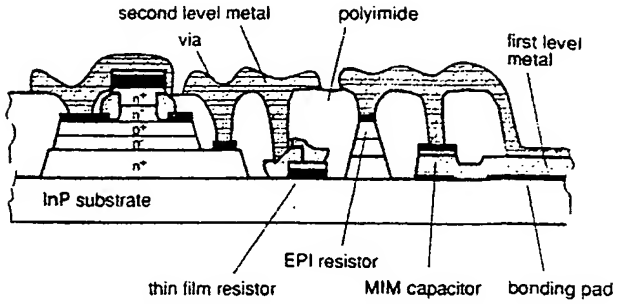


Fig. 5. Cross-section showing the AlInAs/GaInAs HBT process used.

currents in the circuit (cf. Section II).[2] However, this option proved not to be required, due to the good agreement between measurements and simulation prediction. The dc amplifier for the offset control is located in some distance from the amplifier cells. The chip size is 1.6 mm × 1.2 mm.

## IV. Technology Applied

For the fabrication of the IC's, the baseline 3-inch AlInAs/GaInAs HBT process of HRL laboratories was used [6]. The HBT's with AlInAs emitter, GaInAs base, and GaInAs collector achieve 80 GHz for both transit frequency ($f_T$) and maximum oscillation frequency ($f_{max}$). A cross-section of this technology is given in Fig. 5. The process features mesa isolated transistors on a semi-insulating InP substrate, self-aligned base contacts for high-speed operation, thin film TaN resistors and high-resistivity epitaxial resistors, $Si_3N_4$ and polyimide capacitors, and two levels of interconnections. The IC fabrication process constructs the individual HBT's first (typically from $2 \times 2\ \mu m^2$ to $2 \times 20\ \mu m^2$ emitter size), followed by the passive elements. Then the wafers are planarized with polyimide, and vias are formed through the polyimide to expose buried electrodes which are contacted with second level interconnections.

## V. Simulation Results

The simulations of the amplifier were performed with SPICE, however, using an extended transistor model. For example, *two* excess phase delays were implemented in this model (cf. [7]), which proved to be of some influence on circuit behavior and were, therefore, carefully estimated.

Fig. 6 shows the simulated frequency response of the first amplifier cell loaded by the second cell. Plotted are the magnitude $|H|$ and the phase deviation[3] $\Delta\varphi$ of the transfer function $H$ vs. frequency, which is defined by the ratio of the differential output current of the TAS (cf. Fig. 3) to the *intrinsic* current of the PD. As described in Section II, the stage has a comparatively low 3 dB-cutoff frequency for the magnitude (about 20 GHz), but a low phase deviation up to high frequencies. To the authors experience with the design of this and other broadband amplifiers,

[2]This measure is recommended for the first design of an experimental circuit, working at the limit of the technology used (especially, if the technology is still in an experimental state). It allows to compensate for potential technology spread and model inaccuracy so that a redesign can be avoided.

[3]The phase deviation is defined as the difference between the real phase and an "ideal" phase which is proportional to the frequency [8].

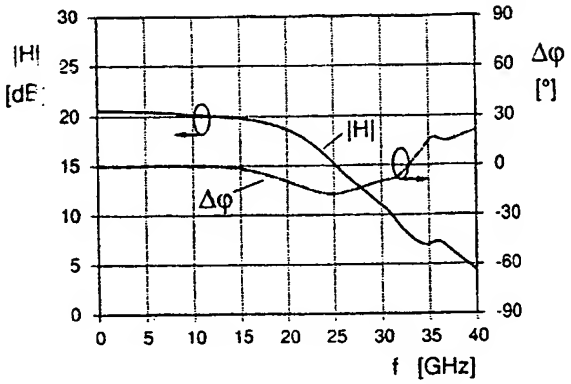


Fig. 6. Simulated frequency response of the first amplifier cell. Shown are the magnitude $|H|$ and the phase deviation $\Delta\varphi$ of the (complex) transfer function $H$ defined in the text.

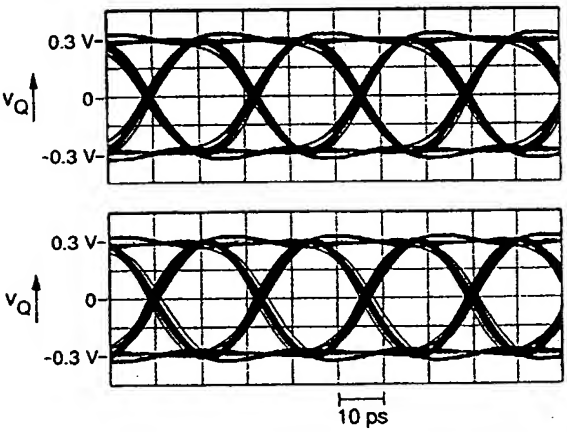


Fig. 7. Simulated output eye diagram at 43 Gb/s for the specified margins of the input current swing $\Delta I_I$. Top: $\Delta I_I = 0.3$ $mA_{pp}$. Bottom: $\Delta I_I = 0.6$ $mA_{pp}$.

the observed $\Delta\varphi$ less than 15° within the frequency range of interest is low enough to guarantee low time jitter.

The simulated eye diagrams at a data rate of 43 Gb/s are shown in Fig. 7. This simulation considers all (known) effects caused by on-chip wiring and substrate coupling as well as by mounting parasitics. The driving PD is modeled by an adequate equivalent circuit [1]. For the transistor parameters target values are used.

## VI. Measurement Results

For measurements, the chip was mounted on a ceramic substrate. Since the ratio of the output voltage $v_Q$ of the amplifier and the *intrinsic* current of the PD ($i_{PD} \propto$ light intensity) is of main interest, in this purely electrical measurement the PD is modeled by a simple equivalent circuit realized on the same substrate. It consists of a high-ohmic thinfilm resistor (500 Ω) approximating a current source,[4] and a thinfilm capacitor (65 fF) which represents the *total* capacitance of the PD. This PD

[4]This assumption was verified by simulations as well as by measurements on a separate thinfilm substrate.

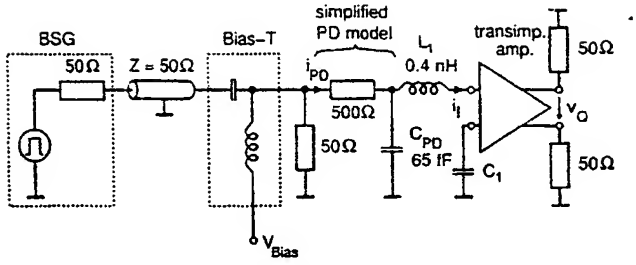


Fig. 8. Circuit diagram of the measurement set-up.

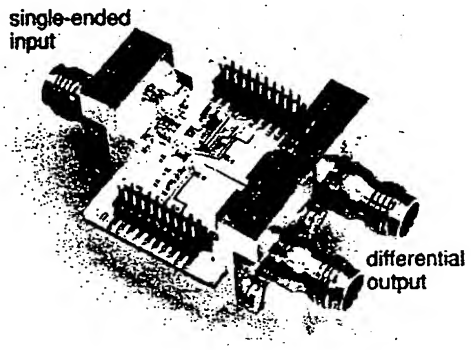


Fig. 9. Photograph of the measurement socket.

model is simplified compared to the model used for circuit simulations. However, the simulation results differs only slightly between both models.

The measurement set-up, shown in Fig. 8, was driven by a quasipseudo-random bit-sequence generator (BSG), developed at Ruhr-University Bochum [9], [10]. For this, four uncorrelated bit sequences of lower data rate, each with a word length of $2^{15}-1$, are multiplexed to a pulse sequence of the desired data rate (for details, see [9]). Between the BSG and the measurement socket, an external bias-T is provided to adjust the input bias voltage of the amplifier. The amplifier output was connected to an HP sampling scope with 50 GHz bandwidth and 50 Ω input impedance.

In Fig. 9, a photograph of the measurement socket is shown, with V-connectors at the single-ended input and at the differential output. The chip is located in a recess of the ceramic substrate, so that the surfaces of the chip and the ceramic substrate are on the same level. This allows us to shorten the length of the bond wires. The external capacitances required for decoupling the unused input terminal and the supply voltage as well as for the low-pass filter in the offset control are all separated in a high-frequency part near the chip and in a lower-frequency part in some distance. Between them, low-ohmic resistors (about 10 Ω) are used to suppress potential oscillation.

The output signal of the BSG, measured behind the bias-T at 50-Ω termination, is shown in Fig. 10. It corresponds to the intrinsic PD current $i_{PD}$ at a swing of $\Delta I_I = 0.3$ $mA_{pp}$. Note, that for this and the following eye diagrams the exposure time was chosen as long as 2 min in order to be sure that the eyes are in fact well opened.

The measurement results presented now were achieved with the first design and the first technological run. The clear output

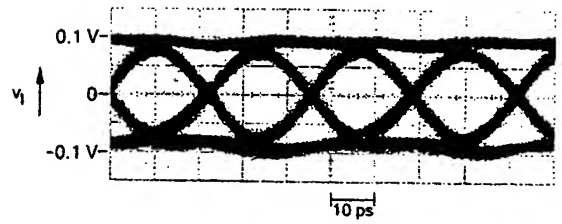


Fig. 10. Input eye diagram at 43 Gb/s, measured at 50 Ω termination behind the Bias-$T$ (cf. Fig. 8). The voltage swing corresponds to an input current swing of $\Delta I_I = 0.3\ \mathrm{mA_{pp}}$.

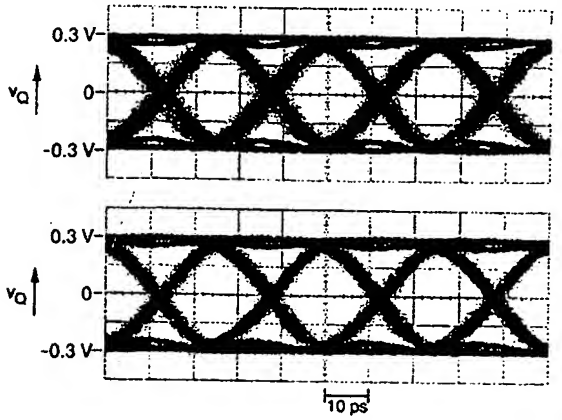


Fig. 11. Measured output eye diagrams at 40 Gb/s for the specified margins of the input current swing $\Delta I_I$. Top: $\Delta I_I = 0.3\ \mathrm{mA_{pp}}$. Bottom: $\Delta I_I = 0.6\ \mathrm{mA_{pp}}$. The differential output voltage swing in both cases is $\Delta V_Q = 0.6\ \mathrm{mV_{pp}}$.

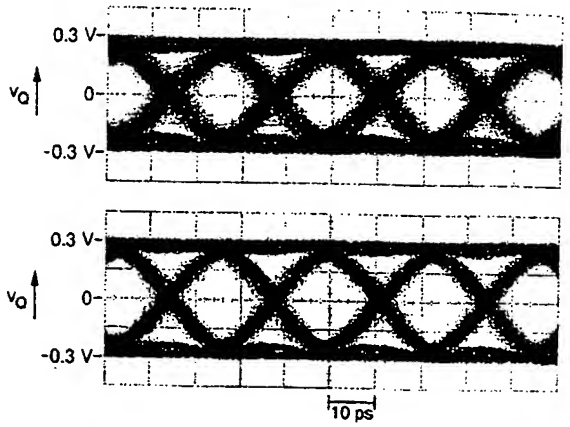


Fig. 12. Measured output eye diagrams at 43 Gb/s for the specified margins of the input current swing $\Delta I_I$. Top: $\Delta I_I = 0.3\ \mathrm{mA_{pp}}$. Bottom: $\Delta I_I = 0.6\ \mathrm{mA_{pp}}$.

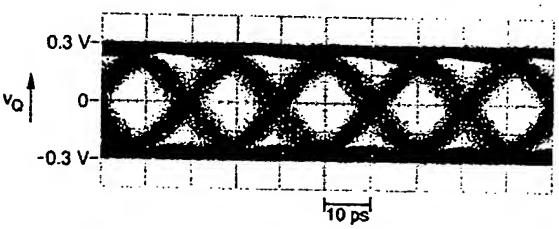


Fig. 13. Measured output eye diagram at 48 Gb/s and $\Delta I_I = 0.6\ \mathrm{mA_{pp}}$, showing the speed limit of the amplifier.

eye diagrams in Fig. 11 were obtained at the nominal data rate of 40 Gb/s for the minimum and the maximum value of the input current swing (top and bottom, respectively). The reliable operation of the offset control was confirmed by changing the bias voltage $V_{\mathrm{Bias}}$ of the bias-$T$ (cf. Fig. 8). No significant influence on the output signal was observed at offset currents up to 1 mA.

Even at 43 Gb/s, well opened eye diagrams with low time jitter were measured within the demanded dynamic range of the input current swing, as shown in Fig. 12. It should be noted that the measurement results in Fig. 12 agree fairly well with the simulation results in Fig. 7 without any readjustments of the currents via bond pads and without reextraction of the transistor parameters (cf. Section V).[5] The smaller eye opening in Fig. 12 (top) compared to Fig. 7 (top) is partly caused by noise in the circuit and the measurement setup, which is not considered in the simulation.

For the upper margin of the input current swing ($\Delta I_I = 0.6\ \mathrm{mA_{pp}}$), even a data rate of 48 Gb/s was reached (Fig. 13), showing the speed limit of the developed amplifier.

## VII. Conclusion

A monolithic integrated transimpedance amplifier for a 40-Gb/s optical-fiber TDM link has been developed. Well opened eye diagrams were measured up to 43 Gb/s for the whole specified input dynamic range and even up to 48 Gb/s for the upper margin of this range. The results confirm that the complete amplifier for a 40-Gb/s receiver can be fabricated in InP-based HBT technology and, despite its high gain, integrated on a single chip. A significant further speed improvement is expected from smaller transistor sizes and a third interconnection level.

[5]However, it should be noted that a reliable check of the simulation accuracy would require a resimulation of the circuit, using transistor parameters extracted from test structures which are located on the same wafer as the measured amplifier sample.

## Acknowledgment

The authors would like to thank M. Pfost (formerly with Ruhr-University Bochum, Germany, now with Infineon Technologies, Munich, Germany) for performing the substrate simulations and A. Schöpflin (Siemens AG, Munich) for developing the measurement socket, as well as M. Edmond and his group (Siemens AG, Munich) for mounting the chips.

## References

[1] H.-M. Rein, "Si and SiGe bipolar IC's for 10 to 40 Gb/s optical-fiber TDM links," in *High-Speed Circuits for Lightwave Communications: Selected Topics in Electronics and Systems*, K. C. Wang, Ed. Singapore: World Scientific, 1999, vol. 1306, pp. 35–71.

[2] J. Müllrich, T. F. Meister, M. Rest, W. Bogner, A. Schöpflin, and H.-M. Rein, "40 Gbit/s transimpedance amplifier in SiGe bipolar technology for the receiver in optical-fiber TDM links," *Electron. Lett.*, vol. 34, pp. 452–453, Mar. 1998.

[3] H.-M. Rein and M. Möller, "Design considerations for very-high-speed Si-bipolar IC's operating up to 50 Gb/s," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1076–1090, Aug. 1996.

[4] M. Pfost and H.-M. Rein, "Modeling and measurement of substrate coupling in Si-bipolar IC's up to 40 GHz," *IEEE J. Solid-State Circuits*, vol. 34, pp. 582–591, Apr. 1998.

[5] M. Pfost, H.-M. Rein, W. Steiner, and A. Stürmer, "Simulation of substrate coupling with special regard to shielding in high-speed Si/SiGe bipolar ICs," in *Proc. 29th Eur. Microwave Conf.*, Munich, Germany, 1999, pp. 133–136.

[6] W. E. Stanchina, J. F. Jensen, R. H. Walden, M. Hafizi, H.-C. Sun, T. Liu, G. Raghavan, K. E. Elliott, M. Kardos, A. E. Schmitz, Y. K. Brown, M. E. Montes, and M. Yung, "An InP-based HBT fab for high-speed digital, analog, mixed-signal and optoelectronic ICs," in *Tech. Dig. GaAs IC Symp.*, 1995, pp. 31–34.

[7] A. Koldehoff, M. Schröter, and H.-M. Rein, "A compact bipolar transistor model for very-high-frequency applications with special regard to narrow emitter stripes and high current densities," *Solid-State Electron.*, vol. 36, pp. 1035–1048, July 1993.

[8] M. Neuhäuser, H.-M. Rein, and H. Wernz, "Low-noise, high-gain Si-bipolar preamplifiers for 10 Gb/s optical-fiber links—Design and realization," *IEEE J. Solid-State Circuits*, vol. 31, pp. 24–29, Jan. 1996.

[9] M. Möller, H.-M. Rein, A. Felder, and T. F. Meister, "60 Gbit/s time-division multiplexer in SiGe-bipolar technology with special regard to mounting and measuring technique," *Electron. Lett.*, vol. 33, pp. 679–680, Apr. 1997.

[10] M. Bussmann, U. Langmann, B. Hillary, and W. W. Brown, "A 12.5 Gb/s Si-bipolar IC for PRBS generation and bit error detection up to 25 Gb/s," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, 1993, pp. 152–153.

**Jens Müllrich** was born in Bad Muskau, Germany, in 1967. He received the Dipl.-Ing. degree from Ruhr-University Bochum, Germany, in 1995.

He joined the research group Semiconductor Devices (Arbeitsgruppe Halbleiterbauelemente), Ruhr-University Bochum as a Research Assistant in 1995. His main field of research is high-speed bipolar IC's, especially amplifiers and frequency dividers.

**Herbert Thurner** was born in Munich, Germany, in 1959. He received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Technical University Munich in 1986 and 1989, respectively.

From 1990 to 1997 he was with Siemens AG, Information and Communication Networks, Munich, where he has worked in the field of broadband ATM switching nodes including design of VLSI circuits and in the development of analog and digital high-speed bipolar IC's for optical communication systems in the multi-gigabit per second range. Since 1997 he has been a Professor in circuit design and microwave engineering at the University of Applied Science Rosenheim, Germany.

**Ernst Müllner** received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from Technical University Munich, Germany, in 1985 and 1990, respectively. His dissertation topic was a study of circuit design principles for BiCMOS technologies.

In 1991 he joined the central lab of the Communication Division, Siemens AG, where he is working on the design of fast bipolar circuits for fiber optic transmission systems for 10 Gbit/s and higher.

**Joseph F. Jensen** (S'81–M'83–SM'92) received the B.S. and M.S. degrees in electrical engineering from the University of California, Los Angeles, in 1980 and 1983, respectively.

In 1981, he joined Hughes Aircraft Company, El Segundo, CA, where his assignments included work on high-speed A/D converters in silicon bipolar technology, VLSI design in CMOS/SOS technology, and testing methodology using electron-beam testing techniques. In 1983, he joined the staff of HRL Laboratories, Malibu, CA, where he is currently a Department Head of the Ultra-High Speed IC Department in the Microelectronics Laboratory. As a member of the Research Laboratories staff, he has been involved with the development of GaAs MESFET's, AlInAs/GaInAs HEMT's, and AlInAs/GaInAs HBT devices and circuits. He is the author of more than 70 papers in the area of high-speed integrated circuits and has received three patents.

Mr. Jensen has served on the ISSCC, IEDM, and IPRM conference program committees. He was an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS.

**William E. Stanchina** (S'69–M'74) received the B.S.E.E. degree from the University of Notre Dame, Notre Dame, IN, in 1971, and the M.S.E.E. and Ph.D. degrees in electrical engineering from the University of Southern California, Los Angeles, in 1975 and 1978, respectively.

He joined the Chemical Physics Department, HRL Laboratories, Malibu, CA, in 1984 after six years as a Member of the Electrical Engineering Department Faculty, University of Notre Dame. He has been involved in research in the following III-V technology areas: surface passivation, gas phase processing, ohmic contacts, and epitaxial and bulk crystal growth. He is currently a Senior Research Scientist and Manager of the Microelectronics Laboratory of HRL Laboratories, responsible for III-V semiconductor research with expertise in the fabrication processes for IC's. He was instrumental in developing the InP-based HBT fabrication technology at Hughes. He is the author or coauthor of more than 50 published articles and has received nine patents with several pending.

Dr. Stanchina is a member of Sigma Xi, Tau Beta Pi, and Eta Kappa Nu. He is a member of the Executive Committee of the IEEE GaAs IC Symposium.

**M. Kardos**, photograph and biography not available at time of publication.

**Hans-Martin Rein** (M'92–SM'99) received the Dipl.-Ing. and Dr.-Ing. degrees in electrical engineering from the University of Stuttgart, Germany, in 1964 and 1968, respectively.

From 1968 to 1973, he worked in the field of advanced integrated circuits (technology and design) for the Semiconductor Division of AEG-Telefunken, Heilbronn, Germany. He was head of the Basic Development of IC's and the MOS Circuits Departments. In 1973 he became a Professor at Ruhr-University Bochum, Germany, where he is teaching integrated circuits. Presently, his main fields of research are high-speed analog and digital bipolar IC's (especially for optical communications) and their fundamental limits, optimization techniques for integrated circuits, as well as modeling of very fast bipolar transistors (including SiGe HBT's) and of on-chip parasitics (e.g. substrate coupling). He is author and coauthor of about 150 technical papers and of a textbook on integrated bipolar circuits.